6 A/D- and D/A-Converter

Physical values change in the macroscopic area always continuously. For the electrical acquisition and processing these values must be converted. The sensor, that converts a physical value into an electrical value, delivers in the general an analog output-signal. The analog signals are acquired by measuring systems, prepared, stored, processed and distributed (transferred).

If high accuracy, high speed and a good price/performance-relationship are needed, these tasks only by digital circuits can be solved.

In complex process-courses and -systems the digital signals must be again converted into analog signals (e.g. in the measuring- and control-engineering).

Analog signals therefore are fed to Analog-to-Digital-Converters (ADC) and digital signals to Digital-to-Analog-Converter (DAC) ("signal-converter").

6.1 Basics of the conversion

The figure DVS-01001 shows for the typical application of an ADC.

A physical value is converted by a sensor into an electrical value. These values are represented by continuous-time and continuous-value signals. The electrical value is converted by an ADC into a digital signal, that is a discrete-value and a discrete-time signal. Only these signals can be processed by a digital system (computer).
After processing in a digital system the results often must be given out, e.g. for controlling of analog processes. So, one need analog signals. These signals are delivered by a DAC (Figure DVS-01002).

The DAC converts the digital signal into an analog signal, which is converted by an actuator into a physical value.

The analog-to-digital conversion in its basic conceptional form is a two-step process: quantizing and coding. Quantizing is the process of transforming a continuous analog signal into a set of discrete output states. Coding is the process of assigning a digital code word to each of the output states.

An ADC compares the input-voltage with his reference-voltages. In the ADC the reference-voltage $U_{\text{REF}}$ is divided into $K$ partial reference-voltages $U_{RQ}$ ("quantums"),

$$U_{RQ} = \frac{U_{\text{REF}}}{K}$$

that are compared with the unknown input-voltage. The number of quantums, that added up delivers the unknown input-voltage, is given out. At binary coding the quantum-measurement is assigned the least significant position of the binary code (= 1 LSB, "Least significant bit"). So the number $K$ of partial reference-voltages at $n$ bit is

$$K \leq 2^n$$

The ADC calculates a binary-number, which represents the quotient out of the input-voltage and the partial reference-voltage. Through the finite partial reference-voltage results an error, because in the general a rest appears. If a finer quantum-measurement is chosen, the error decreases. A high number of output states leads to high resolution. The resolution (= number of the bits $n$) and the maximum speed of conversion characterize the quality of an A/D-converter.
6.2 Parameters of Signal-converters

For the selection of different circuit-principles of signal-converters (ADC respectively DAC) parameters for the determination of quality are given. These parameters not only refer on the resolution or on the maximum speed of conversion. The manufacturers of converters specify values or functions for the static performance in the time- and frequency domain. Some of them will be discussed here; some are listed as a reference.

Static errors:
  - quantization error,
  - linearity,
  - differential linearity,
  - monotony (monotonicity),
  - gain error and
  - offset error.

Dynamic errors:
  - effective number of bits,
  - signal to noise and distortion ratio,
  - spurious free dynamic range and
  - total harmonic distortion.
Quantizer transfer function:
The nonlinear transfer function shows figure DVS-20032. The example shows an ideal quantizer with eight output states and the assigned code words from 000 to 111 (3-bit ADC). The analog input-range for this quantizer is from 0 to $U_{REF}$. There are several important points in the transfer function: seven decision points ($2^3 - 1$) for eight output states ($2^3$). These points or threshold voltages are at

$$(2 \cdot k - 1) \cdot U_{REF}/16.$$ 

The decision points must be precisely set in a quantizer in order to divide the analog voltage range into the correct quantized values. The voltages

$$2 \cdot k \cdot U_{REF}/16$$

are the center points of each output code word. The analog decision point voltages are precisely halfway between the code word center points. The quantizer staircase function is the best approximation which can be made to a straight line drawn through the origin and full scale point. It passes through the center points of all of the code words.

If the input-voltage has both polarities one gets a transfer function as shown in figure DVS-02034:
Quantizer resolution and error:
At any part of the input range of the quantizer, there is a small range of analog values within which the same output code word is produced. This small range is the voltage difference between any two adjacent decision points $U_{RQ}$ (analog quantization size, quantum).

$$U_{RQ} (U_Q; U_{RQ}) = \frac{U_{REF}}{K} = \frac{U_{FS}}{2^n} = \frac{FSR}{2^n} = U_{LSB} (U_{LSB}; LSB)$$

With $U_{FS}$ (U_FS): Voltage of the full scale point
and FSR (FS): Full scale range

Examples: $FSR = 10\, V, n = 3, U_{RQ} = 10\, V / 2^3 = 1,25\, V$
          $FSR = 10\, V, n = 12, U_{RQ} = 10\, V / 2^{12} = 2,44\, mV$

The DAC the resolution is the smallest reproducible alteration of the output-voltage.

The quantizing error is a systematical error, which results from the staircase transfer function between the analog and the digital signal. The error function is like a sawtooth with amplitude $U_{RQ}/2$. It can be reduced only by increasing the number of output states (or the resolution) of the quantizer, thereby making the quantization finer.

The output error varies from 0 to $\pm U_{RQ}/2$. It is only zero at analog values corresponding to the code center points. This error is called quantization uncertainty or quantization error.

Gain error (Full scale error) and offset error:
Real ADC’s and DAC’s require at the analog side amplifiers and comparators. These components show gain- and / or offset-errors. So the transfer function is not ideal. There are three basic deviations from the ideal: offset, gain and linearity, which are all present at the same time in a converter. By external compensation the gain- and the offset-error can be compensated.
Nonlinearity:
The compensation only is made for two points of the transfer function: $X_{DMIN}$ and $X_{DMAX}$. Between these two points remains a deviation from the ideal.

The maximum residual deviation is the linearity error or nonlinearity. The manufacturers use different definitions for the linearity error. The example shows the final point method.

Differential nonlinearity, DNL:
The differential linearity error or differential nonlinearity is defined as the maximum amount of deviation of any quantum from its ideal size of FSR/$2^n$. If the DNL $\geq$ LSB then a code word can be missed (missing code).

Monotony, monotonicity:
The transfer functions must be monotonous. That means that the output of a circuit is a continuously increasing function of the input. Converters may go nonmonotonic if the differential nonlinearity exceeds 1 LSB. DAC’s with non monotonic behaviour can effect in controlling-systems big errors.

Conversion time:
The conversion time consists of two parts:

- the time for quantizing and
- the time for the control of a conversion sequence.

At clocked converters the conversion time can be influenced by the clock frequency. At serial converters the conversion time depends on the input value.
Coding:
The most popular code is the natural binary code (figure DVS-20032) for unipolar converters and for bipolar converters the offset binary code (figure DVS-20034). So the smallest value in each case has the binary value 0. Most converters use unipolar ranges of 0 to 5 V or 0 to 10 V. The standard bipolar ranges are ±2,5 V and ±5 V. Many converters are programmable between these ranges.

Effective Number of Bits (ENOB):
In the section before a number of error effects were discussed. Some of them are (nearly) completely correctable with limited effort like small offset and gain errors. Others are correctable but only with high effort like a monotonic nonlinearity or even uncorrectable like non-monotonicity or missing codes.

How to compare two different ADCs or DACs that have the same number of bits but differ in the error numbers? And what means 10 bit accuracy for a non-ideal device?

The idea is to combine all errors into one error power figure and relate it to the signal power S. The error consists out of the unavoidable quantization noise power N plus the so called distortion power D that includes all other errors. SINAD is the Signal-to-Noise-and-Distortion (power) Ratio:

\[
SINAD = \frac{S}{N + D}
\]

S depends on the amplitude distribution of the signal. The signal power of a sinusoid \( A \cdot \cos(\omega t) \) is \( S = A^2 / 2 \) (bipolar converter) where \( A = \text{FSR}/2 \) is the maximal amplitude. A rectangular signal with amplitudes +/-A has \( S = A^2 \). In praxis nearly always a sine wave voltage is used as test signal because this is the only analog signal that can be generated with sufficient precision. An ideal n-bit ADC has only the quantization error. Using the relation \( A = \text{FSR}/2 = Q \cdot 2^n / 2 \) one can rewrite S:

\[
S = A^2 = \left( \frac{Q \cdot 2^n / 2}{2} \right)^2 = 2^{2n} \cdot \frac{Q^2}{8}
\]

The noise power can be computed with a statistical approach. The error q of the conversion is between -Q/2 and +Q/2, all error values are considered equally likely (acceptable approximation for \( n > 4 \)). In mathematical terms, the probability density function \( p(q) = 1/Q \) is constant for \( |q| < Q/2 \) and 0 elsewhere (DVS-20150).

The expected quantization noise power is than

\[
N = \int_{-\infty}^{+\infty} q^2 \cdot p(q) \cdot dq = \int_{-Q/2}^{+Q/2} q^2 \cdot \frac{1}{Q} \cdot dq = \frac{Q^2}{12}
\]

Using \( N = Q^2 / 12 \) one gets

\[
SNR = \frac{S}{N} = \frac{2^{2n} \cdot \frac{Q^2}{8}}{Q^2 / 12} = 2^{2n} \cdot 1.5 \iff \text{SNR in dB} \approx (n \cdot 6.02 + 1.76) / \text{dB}
\]
For all signals one gets the factor $2^{2n}$ while the factor 1.5 is specific for a sine wave. The number of bits in the ideal case is therefore related to the SNR by

$$n = \frac{\text{SNR} \, / \, \text{dB} - 1.76}{6.02}$$

The ENOB for a sinusoid test signal is defined based on that equation:

$$\text{ENOB} = \frac{\text{SINAD} / \, \text{dB} - 1.76}{6.02}$$

For the ideal n Bit ADC is $D = 0$ and one gets $\text{ENOB} = n$. When the distortion increases the SINAD and ENOB decrease. Two ADC have the same number of effective bit if they generate the same SINAD. The signal quality is the same if SINAD is the metric. This is in many applications a very sensible and meaningful definition. Note that having a sinusoid means we have also a frequency. ENOB is frequency dependant. In a data sheet the function is given as a plot or a worst case value. An alternative is to specify the minimum SINAD.

Some notes
1) Sometimes one finds SNR in the ENOB definition instead of SINAD. This is due to the interpretation of all effects as noise. SNR means than the same as SINAD. This imprecise notation should be avoided.
2) In the literature the terms SNR and SINAD are mixed with their values in dB. One must look at the equations to avoid errors and confusion.
3) We have tooked of ENOB only for ADC but not for DAC. The latter is often missing in the literature, but it is also possible to define ENOB for a DAC. The measuring of SINAD for a DAC in the time domain is complicated, but no problem in the frequency domain (spectral analyzer).
4) Remember that in the derivation of ENOB a full-scale input sine wave was assumed. If the signal level is reduced, the S and therefore SINAD and ENOB decrease.
5) The (Signal to Noise Distortion Ratio) is sometimes abbreviated SNDR instead of SINAD.
**Spurious Free Dynamic Range (SFDR)**

The SFDR (Spurious Free Dynamic Range) indicates in dB the distance between the powers of the signal or the maximum power and the strongest spurious.

These figures are mostly given as dB values, SFDR in dBc is more common. Note that the SFDR in dBc is an upper limit for the SINAD. It is the dominant error for modulation or demodulation applications in communication.

### 6.3 Circuits for the analog signal-processing and -distribution

The figure DVS-20510 shows the most important components to the analog signal-processing and -distribution. Input amplifiers for the adaption of the levels and converting of the impedance, active filters for the reduction of the frequency range and analog multiplexers for the input of different analog input channels. A sample & hold circuit acquires the input value and holds it while the ADC converts it into digital form. Then the signal is processed digitally and given out by a DAC with reconstruction-filters and output-amplifiers. Figure DVS-20610 shows the principle of an analog MUX. It consists out of transmission gates and a decoder (1 of J).
INPUT AMPLIFIER

FILTER

ANALOG-MUX

S&H

A/D

DIGITAL PROCESSING

OUTPUT AMPLIFIER

RECONSTRUCTION FILTER

Proc. Dr. J. Vollmer

Prof. Dr. F. Schubert

University of Applied Sciences
Hamburg

DVS-20510

PROCESSING AND DISTRIBUTION OF SIGNALS

X1

1

1

U_E1

U_E2

U_EJ

X/Y

DECODER

X1

1

1

X1

1

1

TRANSMISSION-GATES

U_A

Prof. Dr. F. Schubert
University of Applied Sciences
Hamburg

DVS-20610

PRINCIPLE OF AN ANALOGUE MUX
A sample & hold circuit on principle consists out of a switch and a capacitor (DVS-30001):

![Sample & Hold Circuit Diagram]

The sample & hold circuit is an analog memory with high precision and stability. While a very short phase of sampling it is picked up the analog input-signal. The last value of sampled signal is stored in the hold-phase in a capacitor. Input- and output-amplifiers care for a decoupling of the hold-capacitor. This circuit has two main tasks:

1.) It delivers time constant input-signals for ADC’s with long conversion time.

2.) The time of the signal-storage is fixed exactly by the H/L-edge of the control signal.

The equivalent circuit is shown at the bottom of figure DVS-30001. It consists of a real switch with two finite resistors, a finite load at the output and a real input voltage source.

### 6.4 Procedures and circuits of the D/A-conversion

Digital-to-analog-converters deliver at the output an analog signal in dependence on a digital input-signal (data-word). The analog output-signal is the product out of the quantum for 1 LSB and the dual number at the input. DACs with external reference-voltage therefore also are called "multiplying DACs".

For the D/A-conversion three different types are popular: two parallel types with equal resistors (or current-sources) and with dual weighted resistors (or current-sources) and a serial procedure with capacitors (in switched-capacitor-technology), that for definite intervals are charged or discharged.

The selection of a principle is dependent on the resolution, the converting speed, the circuit-integration and the appearing errors. An important parameter, that only appears at DACs,
the glitch at the output, that appears at the change of the input-value, if the switches not switch at the same time. It is an essential measurement for the quality of a DAC.

### 6.4.1 D/A-Converters with equal resistors or current-sources

At this type quantum are generated from a voltage or current source. The voltage-quantums are generated by a simple voltage-divider (DAU-01001).

The switches can be analog-MUXs, which are controlled by a decoder (1-of-k). Only one switch can be conducting at a time. So one gets four different voltages at the output:

\[ U_A = M \times \frac{U_{REF}}{k} \quad \text{with} \quad 0 \leq M \leq k-1 \]

For a n-bit DAU one needs \( k = 2^n \) resistors and switches.

### 6.4.2 D/A-converters with weighted resistors or current-sources

If one uses weighted resistors, for n bit only n resistors and switches are needed. The basic circuit for dual-weighted resistors shows figure DAU-01002. The resistor R belongs to the MSB (Most significant bit) of the n-bit wide data-word. At \( Z_J = "1" = \text{HIGH} \) the switch connects the resistor with the reference-voltage \( U_{REF} \), at \( Z_J = "0" = \text{LOW} \) the switch connects the resistor with ground. Because of the different voltage-dividers this 3-bit-DAC generates all voltages between \( U_A = 0 \) V and \( 7/8 \) \( U_{REF} \) with \( U_{LSB} = 1/8 \) \( U_{REF} \). A realization with an Opamp shows figure DAU-01020.
Through the weighted resistors flow weighted currents in dependence on the switch-positions (Z₃ until Z₀), that at the inverting input are added and flow through the resistor R to the output. The output-voltage is:

\[ U_A = -U_{REF} \times \left( \frac{1}{8} Z_0 + \frac{1}{4} Z_1 + \frac{1}{2} Z_2 + \frac{1}{1} Z_3 \right) \]

with \( Z_i = 0 \) or 1.
Because of the difficulty to manufacture weighted resistors on a chip another principle of weighting is used: the R-2R ladder method (DAU-01030):

The operation of the R-2R ladder network is based on the binary division of the current as it flows down the ladder. A looking to the right of every point of the ladder one measures a resistor of R. So the reference-voltage is always divided by two and through the switches flow weighted currents that are summed at the inverting input of the Opamp. The current I is:

\[ I = \frac{U_{\text{REF}}}{2R} \times \left( \frac{1}{8} Z_0 + \frac{1}{4} Z_1 + \frac{1}{2} Z_2 + \frac{1}{1} Z_3 \right) \]

with \( Z_i = 0 \) or \( 1 \).

### 6.4.3 SC-converter

The SC-Converter (Switched Capacitor Converter) is a serial converter with switched capacitors. Two capacitors \( C_1 = C_2 = C \) are cyclic charged or uncharged (DST-01003).

At the beginning of a conversion both capacitors are uncharged. The clock is divided in two clock phases \( T_0 \) and \( T_1 \). The conversion starts with the LSB. In clock phase \( T_0 \) the switch \( S_0 \) is in position 1, if the LSB = "1" (the capacitor is charged with \( U_{\text{REF}} \)) or in position 0, if the LSB = "0". The switch \( S_1 \) is in position 0.

In clock phase \( T_1 \) the switch \( S_0 \) is in position 2 and \( S_1 \) in position 1. So the charge will be divided to the two capacitors and the voltage decreases to the half.

During the next clock in clock phase \( T_0 \) the switch \( S_0 \) is in position 1 or 0 (depending on the next bit value). This effects in clock phase \( T_1 \) a charge balancing between \( C_1 \) and \( C_2 \) and the voltage at capacitor \( C_2 \) becomes \( U_A = U_{C_2} = Q_{C_2}/C_2 \). Figure DAU-01004 shows the voltages \( U_A \) at the capacitor \( C_2 \) for the serial word 101.
SC-CONVERTER

U_{REF}

C

S_0

S_1

U_A

OUTPUT-VOLTAGE

U_A

U_{REF}

5/8 U_{REF}

1/2 U_{REF}

1/4 U_{REF}

0

1

0

1

LSB

MSB

DAU-01003

DAU-01004
6.5 Procedures and circuits of the A/D-conversion

Analog-to-digital-converter employ a variety of different circuit techniques to implement the conversion function. The most important types are:

- parallel ADC (flash ADC)
- two-stage parallel ADC
- serial ADC and
- slope ADC.

6.5.1 Parallel ADC

The parallel converter ("Flash converter") is the fastest ADC. One generates through voltage dividers $2^n-1$ partial reference-voltages that are at the inputs of comparators. The other inputs of the comparators are at the input-voltage $U_E$ (ADU-02010).

For the quantum-size is valid

$$U_{RO} = U_{LSB} = U_{REF}/(2^n-1)$$

Clocked registers store the data of the outputs of the comparator (e.g. by the positive edge). The states of the output of the comparators and the flip-flops depend on the input-voltage $U_E$:

<table>
<thead>
<tr>
<th>Q7</th>
<th>Q6</th>
<th>Q5</th>
<th>Q4</th>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
<th>$U_E/(U_{REF}/14)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>&lt; 3 and &gt; 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>&lt; 11 and &gt; 9</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>&lt; 13 and &gt; 11</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>&gt; 13</td>
</tr>
</tbody>
</table>

- 121 -
Is \( U_E \) for example between 5/14 \( U_{REF} \) and 7/14 \( U_{REF} \), so the outputs of K1 until K3 have HIGH-level (K4 until K7 have LOW). So one gets eight different states, that are represented by the three bits \( Z_2, Z_1 \) and \( Z_0 \). A 7-to-3-decoder converts the output code into the binary code.

These ADCs are very fast (Sampling frequencies until to the GHz range). The accuracy of the resistors limits the resolution of the converters. Now 8-bit-converters are the standard. The manufacturing of 10-bit-converters has high technological difficulties. Because of the register an analog sample&hold-circuit is not necessary.

The number of resistors is \( 2^n \) and the number of comparators is \( 2^n-1 \). A 4-bit converter, for example, requires only 15 comparators, but an 8-bit converter needs 255. For this reason it is common practice to implement an 8-bit A/D with two 4-bit stages.

### 6.5.2 Two-stage parallel A/D-Converter

To the avoidance of the high number of resistors and comparators two-stage parallel A/D-converter ("half-parallel or Semi flash converter") is used. At this cascade-procedure one distinguishes between a coarse- and fine-quantization (ADU-02020).

A parallel ADC (ADC1) is used for the coarse-quantization of \( n/2 \) bits. In a second step the result is converted back to analog by means of an ultra-fast 4-bit DAC. The output-voltage \( U_{DAC} \) of the DAC is subtracted from the input-voltage \( U_E \). The resulting difference \( U_E-U_{DAC} \) then is converted by the second ADC (ADC2). At the output the two data sets are accumulated in a register. During the conversion time the input-voltage might not change. A sample & hold circuit is to implement.

The advantage of this circuit is the low number of comparators. Only \( 2*(2^{n/2}-1) \) comparators, one differential amplifier and an \( n/2 \)-Bit-DAC are required. Disadvantages are the longer conversion time and the appearance of linearity errors (e.g. not monotonous behavior,
"missing codes"). To remove these disadvantages a digital error-correction with the increase of the word-width of ADC2 is used. During the conversion time of the ADC2 the ADC1 can process the next coarse-quantizing. This "pipelining" accelerates the conversion.

### 6.5.3 Serial A/D-Converter

The most popular A/D conversion technique in general use for moderate to high speed application a serial type ADC, the successive-approximation ADC. This method falls into the class of feedback type converters. In these cases a DAC is in the feedback loop of a digital control circuit which changes his output until it equals the analog input.

In the case of the successive-approximation, the DAC is controlled in an optimum manner to complete a conversion in \( n \) steps for an \( n \)-bit converter. The operation is like an weighting procedure using standard weights in a binary sequence (1, \( \frac{1}{2} \), \( \frac{1}{4} \), ..... , \( \frac{1}{n} \)). First the largest weight is placed on the balance pan. If it does not tip, the weight is left on and the next largest weight is added. If the balance does tip, the weight is removed and the next one added. The procedure is used for the next largest weight and so on down to the smallest.

The circuit (ADU-02030) exists out of a sample & hold circuit, a comparator, a DAC and a register for the successive approximation register ("SAR").

At this ADC the input-voltage \( U_E \) is compared with the output-voltage \( U_{DAC}(Z) \) of the internal DAC. The SAR controls the DAC by implementing the weighting logic as described. First the SAR turns on the MSB of the DAC and the comparator tests this output against the analog input. The decision signal \( D \) is made by the comparator to leave the bit on or to turn it off. After this the next bit is turned on and a second comparison is made. After \( n \) comparisons the output of the SAR indicates all bits which remain.

The figure ADU-02032 shows the sequence of successive-approximation for three bits.
If the SAR is changed against an up/down-counter, so the counter increases his number until the output-voltage of the DAC equals the input-voltage (ADU-02040).

Because of the feedback the output-voltage of the DAC follows the input-voltage $U_E$ ("Tracking ADC"). The output of the counter is the data-word. The converter is very slow; the conversion time is not constant and depending on the value of the input-voltage. This procedure is used at digital voltmeters.
6.5.4 A/D-Converter with ramp-procedure

If the ramp is generated analog by integrators, one speaks of "ramp-procedure". The simplest ramp-procedure with one ramp ("single slope") compares the input-voltage with a sawtooth voltage \( U_R(t) \) (ADU-02050).

![Diagram of A/D Converter with Ramp Procedure](image_url)

The impulses of a quartz-generator are at the input of a gate, that is open from the time where \( U_R(t) \) crosses zero until \( U_R(t) \) equals the input-voltage. The number of the counted impulses is proportional to the input-voltage. The ramp-generator must have a high linearity and long-time-stability. The expenditure for an analog circuit with a stable reference-voltage for generating the ramp-voltage is very high, so this circuit is not more used.

There is a different situation if one takes a second phase of integration. Then long-time-stability-influences are compensated. The integrator only must be stable during the conversion time. At this double-ramp ADC ("Dual slope-ADC") the input-voltage is integrated for a fixed time \( T_1 \) (ADU-02060).

During the time \( T_1 \) \( N_1 \) impulses with a period \( T \) appear. The counter counts up to overflow. At this point the control circuit switches the integrator to the negative reference voltage \( U_{REF} \), which is integrated until the output is back to zero. The clock pulses are counted during this time \( T_2 \) until the comparator detects the zero crossing and turns them off. The number of counted pulses is \( N_2 \):

\[
N_2 = \frac{T_2}{T}
\]

The phases of integration for different input-voltages shows figure ADU-02061.
At the start of the measurement the switch $S_3$ is opened and $S_1$ is closed. The output voltage of the integrator is:

$$U_1(T_1) = -\frac{1}{R \cdot C} \int_0^{T_1} U_E(t) \, dt$$
If $U_E$ is constant during $T_1$, one gets:

$$U_I(T_1) = -(U_E \cdot T_1) / (RC)$$

For the integration of $U_{\text{REF}}$ one gets ($S_1$, $S_3$ opened and $S_2$ closed):

$$U_I(T_2) = -\frac{1}{RC} \int_{0}^{T_2} U_{\text{REF}} dt$$

$$U_I(T_2) = (U_{\text{REF}} \cdot T_2) / (RC)$$

With $U_I(T_1) + U_I(T_2) = 0$ V follows

$$U_E = U_{\text{REF}} \cdot T_2 / T_1$$

$$U_E = U_{\text{REF}} \cdot N_2 / N_1$$

This result shows that the conversion accuracy is independent on the stability of the clock and the time-constant $RC$ so long as they are constant during the conversion period. An offset error of the integrator can be avoided by using a null balance ("Quad slope-ADC") (ADU-02065).

The offset-voltage is integrated, stored in a capacitor. In the conversion phase the stored voltage is subtracted from the input voltage.