Task 5

DCC
Digital Command Control

Control of Model Trains
The NMRA baseline digital command control signal consists of a stream of transitions between two equal voltage levels that have opposite polarity. Alternate transitions separate one bit from the next. The remaining transitions divide each bit into a first part and a last part. Digital Command Stations shall encode bits within this digital command control stream of transitions by varying the duration of the parts of the bits, or frequency of the transitions.

In a "1" bit, the first and last part of a bit shall have the same duration, and that duration shall nominally be 58 μs, giving the bit a total duration of 116 μs. Digital Command Station components shall transmit "1" bits with the first and last parts each having a duration of between 55 and 61 μs. A Digital Decoder must accept bits whose first and last parts have a duration of between 52 and 64 μs, as a valid bit with the value of "1".

In a "0" bit, the duration of the first and last parts of each transition shall nominally be greater than or equal to 100 μs. To keep the DC component of the total signal at zero as with the "1" bits, the first and last part of the "0" bit are normally equal to one another. Digital Command Station components shall transmit "0" bits with each part of the bit having a duration of between 95 and 9900 μs with the total bit duration of the "0" bit not exceeding 12000 μs. A Digital Decoder must accept bits whose first or last parts have a duration of between 90 and 10000 μs as a valid bit with the value of "0". The figure provides an example of bits encoded using this technique.

Digital Decoders must accept one bits whose positive and negative components differ by as much as 6 μs.
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### For Power Station Output under Load:

<table>
<thead>
<tr>
<th>Relationship for One Bits</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period A &lt; 55 μs or Period A &gt; 61 μs</td>
<td>Bad</td>
</tr>
<tr>
<td>Period A = Period B</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>Period A – Period B</td>
</tr>
<tr>
<td></td>
<td>Period A – Period B</td>
</tr>
</tbody>
</table>

**Decoders must accept:**

<table>
<thead>
<tr>
<th>Relationship for One Bits</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period A &gt;= 52μs and Period A &lt;= 64 μs</td>
<td>OK</td>
</tr>
<tr>
<td>Period A = Period B</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>Period A – Period B</td>
</tr>
</tbody>
</table>
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Preamble: The preamble to a packet consists of a sequence of "1" bits. A digital decoder must not accept as a valid, any preamble that has less then 10 complete one bits, or require for proper reception of a packet with more than 12 complete one bits. A command station must send a minimum of 14 full preamble bits.

Packet Start Bit: The packet start bit is the first bit with a value of "0" that follows a valid preamble. The Packet Start Bit terminates the preamble and indicates that the next bits are an address data byte.

Address Data Byte: The first data byte of the packet normally contains eight bits of address information. The first transmitted address bit shall be defined to be the most significant bit of the address data byte. Address Data Bytes with values 00000000, 11111110, and 11111111 are reserved for special operations and must not be transmitted except as provided in this Standard or associated Recommended Practices.

Data Byte Start Bit: This bit precedes a data byte and has the value of "0".

[Data Byte: Each data byte contains eight bits of information used for address, instruction, data, or error detection purposes. The first transmitted data bit of each data byte shall be defined to be the most significant bit of the data byte.]

Packet End Bit: This bit marks the termination of the packet and has a value of "1".

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The Baseline Packets are included to provide the minimum interoperability between different systems.

**Speed and Direction Packet For Locomotive Decoders**

<table>
<thead>
<tr>
<th>Preamble</th>
<th>Byte One</th>
<th>Byte Two</th>
<th>Byte Three (Error Detection Data Byte)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111111111</td>
<td>0AAAAAAA</td>
<td>01DCSSSS</td>
<td>EEEEEE1</td>
</tr>
</tbody>
</table>

**Byte One:** Address Data Byte = 0AAAAAAA The address data byte contains the address of the intended recipient of the packet. Every Digital Decoder shall be capable of retaining and recognizing its own address for purposes of responding to Baseline Packets. Locomotive Digital Decoders shall support the full range of baseline addresses in such a manner that this address is easily configurable by the user. It is acceptable for Digital Command Stations to restrict the number of valid addresses supported so long as this restriction is clearly and plainly labeled on the package and in the instructions.

**Byte Two:** Instruction Data Byte = 01DCSSSS The instruction data byte is a data byte used to transmit speed and direction information to the locomotive Digital Decoder. Bits 0-3 provides 4 bits for speed (S) with bit 0 being the least significant speed bit. Bit four of byte 2 (C) by default shall contain one additional speed bit, which is the least significant speed bit. For backward compatibility, this bit may instead be used to control the headlight. This optional use is defined in RP-9.2.1. Bit 5 provides one bit for direction (D). When the direction bit (D) has a value of "1" the locomotive should move in the forward direction. A direction bit with the value of "0" should cause the locomotive to go in the reverse direction. Bits 7 and 6 contain the bit sequence "01" which are used to indicate that this instruction data byte is for speed and direction.
### Digital Decoder Reset Packet For All Decoders

<table>
<thead>
<tr>
<th>Preamble</th>
<th>Byte One</th>
<th>Byte Two</th>
<th>Byte Three (Error Detection Data Byte)</th>
</tr>
</thead>
<tbody>
<tr>
<td>111111111111</td>
<td>000000000 0</td>
<td>00000000 0</td>
<td>00000000 1</td>
</tr>
</tbody>
</table>

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![Image](image_url)
# L293E

## MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vs</td>
<td>Supply Voltage</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Vss</td>
<td>Logic Supply Voltage</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Vi</td>
<td>Input Voltage</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Vinh</td>
<td>Inhibit Voltage</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Iout</td>
<td>Peak Output Current (non repetitive $t = 5\text{ms}$)</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>Ptot</td>
<td>Total Power Dissipation at $T_{\text{ground-pins}} = 80°C$</td>
<td>5</td>
<td>W</td>
</tr>
<tr>
<td>Tstg, Tj</td>
<td>Storage and Junction Temperature</td>
<td>–40 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>
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